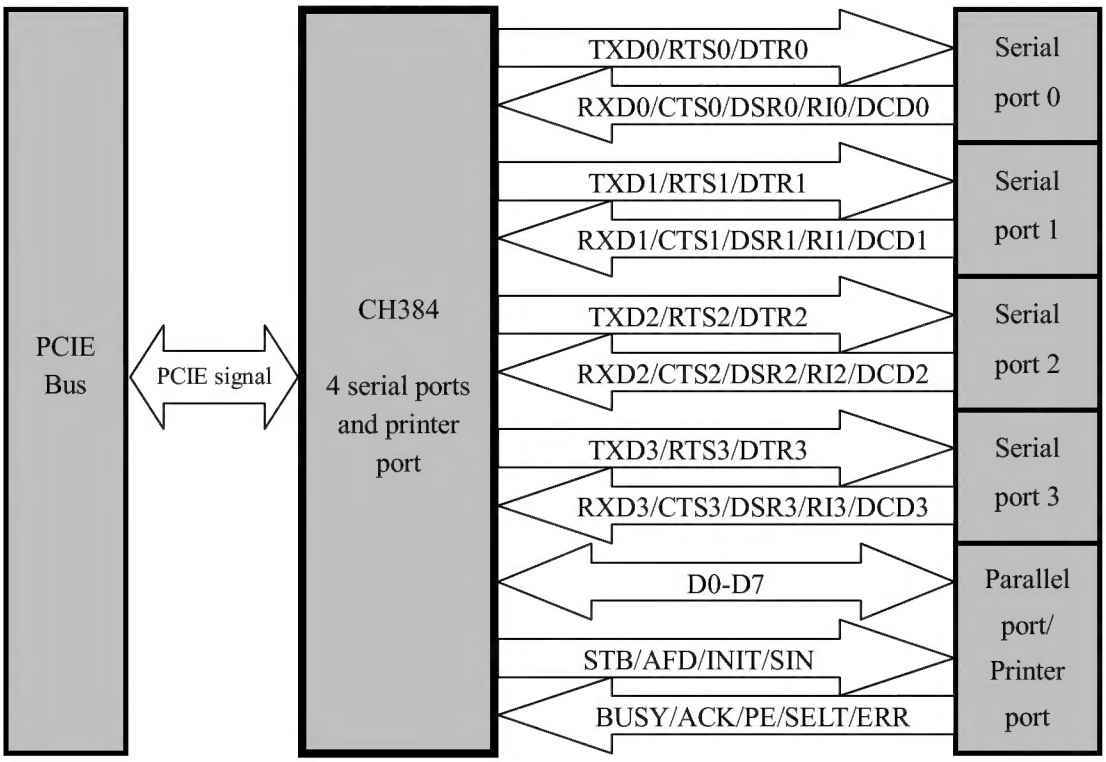
PCIE Bus Quad Serial Ports and Printer Port Chip CH384

Brief (I)
Version: 1
http://wch.cn

1. Introduction

CH384 is aPCI-Express bus converter chip, which converts PCIE bus to Quad serial ports and printer port, including four asynchronous serial ports compatible with 16C550 or 16C750, and one EPP/ECP enhanced bidirectional parallel port.CH438 chip can be added to extend 24 serial ports to the maximum. The asynchronous serial port provides a transceiver with independent 256-byte FIFO buffer, supports IrDA infrared encoding and decoding, supports communication baud rate up to 8Mbps and can be used for RS232 serial port expansion of PCIE bus, PCIE high-speed serial port with automatic hardware flow control, serial ports networking, RS485 communication, IrDA communication, parallel/printer port expansion, etc.

The figure below shows its general application block diagram.



2. Features

2.1. Overview

- The same chip can be configured as a four-channel serial ports and a parallel port/printer port or four-channel serial ports and extended multiple serial ports of PCIE Bus.
- Provides two-wire serial host interface, and EEPROM device similar to 24C0X which can be connected to store non-volatile data.
- The device identification (Vendor ID, Device ID, Class Code, etc.) of the PCIE board can be set in the EEPROM device.
- Drivers support Windows 98/ME/NT4.0/2000/XP/Vista/7/8/8.1/10/SERVER 2003/2008/2012/2016/2019and Linux.
- 3.3V power supply, I/O pins supports 5V withstand voltage, serial ports support low-power sleep

mode.

- The chip function is equivalent to CH367 with CH438, provide such application solutions as 8 serial ports, 16 serial ports and 28 serial ports.

2.2. Serial Port

- 4 fully independent asynchronous serial ports, compatible with 16C550, 16C552, 16C554 and 16C750 and enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Supports odd, even, mark, space and no parity. .
- Programmable communication baud rate, supports communication baud rate of 115200bps and up to 8Mbps.
- Internal 256-byte FIFO buffer, supports four FIFO trigger levels.
- Supports MODEM interface signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 signals.
- Supports automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Supports serial port frame error detection and Break line interval detection.
- Supports full-duplex and half-duplex UART communication.
- Internal SIR infrared codec of serial port 0, supports IrDA infrared communication with baud rate from 2400bps to 115200bps.
- Supports to connect to external CH438 chips to expand another 8 to 24 asynchronous serial ports to realize 8 to 28 serial ports of PCIE.

2.3. Parallel Port

- Supports SPP, Nibble, Byte, PS/2, EPP, ECP and other IEEE1284 parallel port/printer port working modes.
- Supports bidirectional-data transmission and a transmission speed of up to 1M byte/s.

3. Package

Package	Width of Plastic	Pitch of Pin		Instruction of Package	Ordering Information
LQFP-100	14mm x 14mm	0.5mm	19.7mil	Standard LQFP 100 patch	CH384L

4. Configuration

4.1. Global Function Configuration

CH384 has two main hardware function modes: 4 serial ports and parallel port function mode, 4 serial ports and extended multiple serial ports function mode. The pin definitions are different in two function modes, and this manual only covers the former. Please refer to Datasheet (II) CH384DS0_2.PDF for the latter.

4S1P# pin of CH384 is used to select the software recognition mode:

4S1P# is connected to VCC33 or suspended, that is, when 4S1P#=1, it is 4 serial ports mode (parallel port/printer port is not used);

4S1P# is connected to GND, that is, when 4S1P#=0, it is 4 serial ports and printer port mode.

CKSEL pin of CH384 is used to select the clock frequency of the internal 4 serial ports:

CKSEL is connected to VCC33 or suspended, i.e. when CKSEL=1, the clock is input from XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient is 1/12 frequency

division by default, and frequency doubling can be selected through CK2X or CKnS;

CKSEL is connected to GND, that is, when CKSEL=0, the clock is input from XO pin. The frequency is determined by the external crystal, and the internal frequency coefficient is always forced to be frequency doubling;

CKSEL is connected to PERST# pin, that is, when CKSEL=R, the internal crystal oscillator is disabled, the internal PLL provides the clock with a frequency of 125MHz, and the internal frequency coefficient is 1/68 frequency division by default, and supported to selectno frequency division through CK2X or CKnS.

4.2. External Configuration Chip

CH384 will check the data in the external 24CXX configuration chip after each power-on or PCIE Bus reset. If the configuration chip is connected and the data is valid, it will be automatically loaded into CH384 to replace the default PCIE identification information.

The following table shows the data definition in the configuration chip 24CXX.

Byte address	Abbreviation	Description of Chip Configuration Data Area	Default
00H	CFG	The valid flag of the external configuration chip, must be 54H	54H
01H	FREQ	Bit 3 to bit 0are respectively used to select the internal frequency coefficient of serial port 3 to port 0	0FFH
03H-02H	RSVD	(Reserved)	0000H
05H-04H	VID	Vendor ID	Customize
07H-06H	DID	Device ID	Customize
08H	RID	Chip version: Revision ID	Customize
0BH-09H	CLS	Device type code: Class Code	070005H
0DH-0CH	SVID	Subsystem Vendor ID	Customize
0FH-0EH	SID	Subsystem ID	Customize
1FH-10H	RSVD	(Reserved)	00H or FFH
Other address	APP	User or application program custom unit	

5. Applications

5.1. Quad Serial Ports + Parallel Port (Figure below)

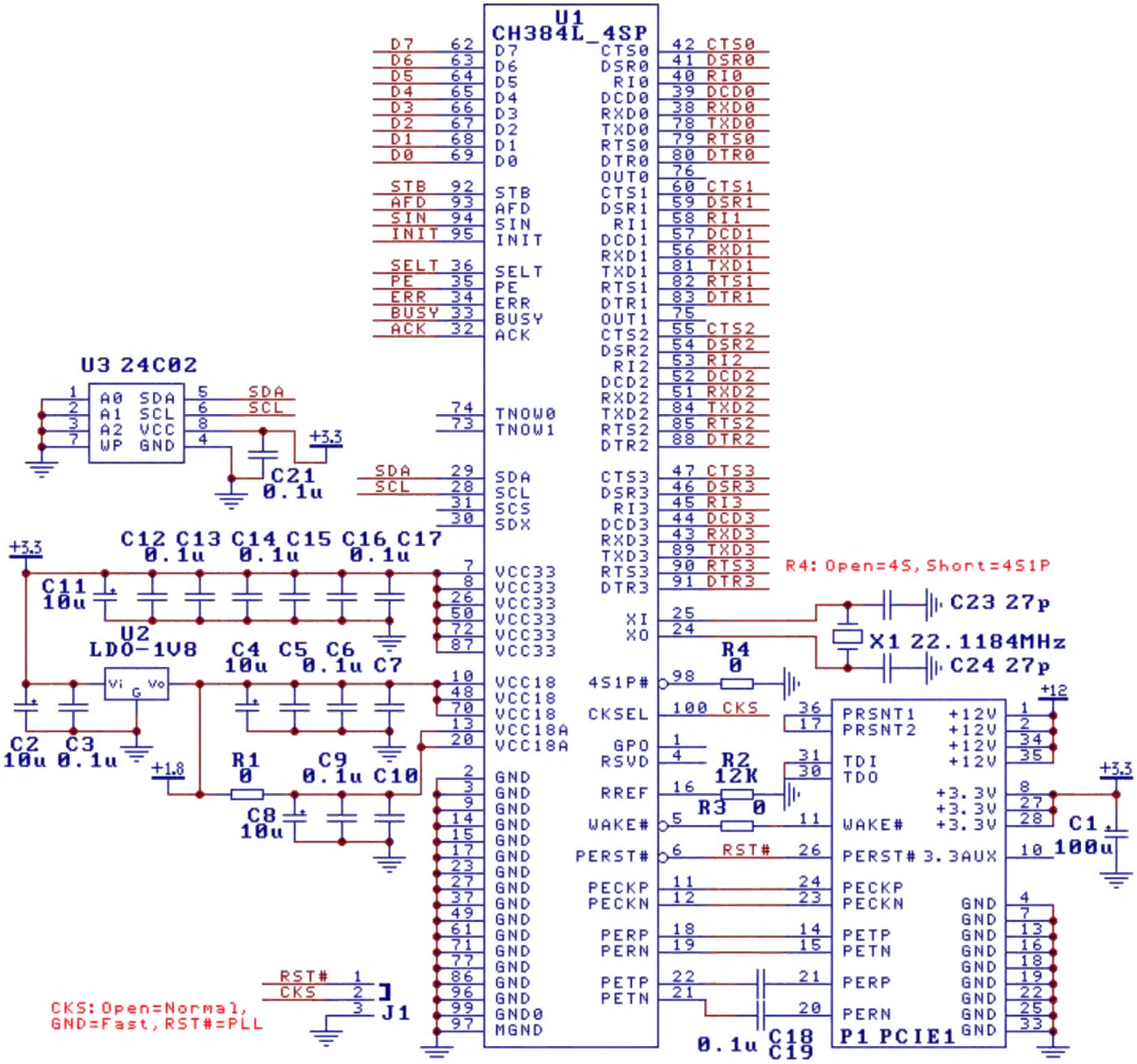
This is the basic circuit for PCIE quad serial ports + parallel/printer port based on CH384. The figure does not include RS232 voltage conversion chip.

U3 is an optional external configuration chip, and the online configuration tool software for Windows system is available on the website.

IEEE1284 requires the printer port signals to keep impedance matching. Therefore, the parallel data singals of the printer port may be connected to resistors in series and capacitors in parallel, which can also be eliminated when the requirement is not high.

Crystal X1, capacitors C23 and C24 are used in the clock oscillation circuit. Other capacitors are used for power supply decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are connected in parallel to the power pins of CH384 respectively.

CH384 is a high frequency circuit. Please refer to PCIE Bus specification or PCIE_PCB.PDF document when designing the PCB board.


U1
CH384L_4SP
U3 24C02
A0 SDA
A1 SCL
A2 VCC
WP GND
SDA
SCL
+3.3
C21
0.1u
C12 C13 C14 C15 C16 C17
0.1u 0.1u 0.1u
C11
10u
U2
LDO-1V8
Vi G Vo
C4 C5 C6 C7
10u 0.1u
C2 C3
10u 0.1u
+1.8
R1
0
C9
0.1u C10
C8
10u
+12
R4: Open=4S, Short=4S1P
C23 27p
X1 22.1184MHz
C24 27p
R4
0
R2
12K
R3 0
RST#
CKS
C1
100u
PRSNT1 +12V
PRSNT2 +12V
TDI
TDO
WAKE#
PERST# 3.3AUX
PECKP
PECKN
PETP
PETN
PERP
PERN
P1 PCIE1
0.1u C18
C19
RST#
CKS
J1
CKS: Open=Normal,
GND=Fast, RST#=PLL